REMARKS

The Official Action mailed July 24, 2008, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on March 18, 2004; October 24, 2007; and April 22, 2008.

A further Information Disclosure Statement is submitted herewith and consideration of this Information Disclosure Statement is respectfully requested.

Claims 1-31 are pending in the present application, of which claims 1-5, 7-9, 11-13 and 23-25 are independent. Claims 2-5, 8, 9, 12, 13 and 15-22 have been withdrawn from consideration by the Examiner (Box 4a, Office Action Summary, page 2, Paper No. 20080718). Accordingly, claims 1, 6, 7, 10, 11, 14 and 23-31 are currently elected, of which claims 1, 7, 11 and 23-25 are independent. Claims 1, 7, 11 and 23-25 have been amended to better recite the features of the present invention. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 8 of the Official Action rejects claims 1, 6, 7, 10, 11, 14 and 23-31 as obvious based on the combination of U.S. Patent No. 6,774,877 to Nishitoba and U.S. Patent No. 6,359,606 to Yudasaka. The Applicant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the

prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. The independent claims have been amended to clarify that a first transistor and a second transistor share a same semiconductor layer. For the reasons provided below, Nishitoba and Yudasaka, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

The Official Action concedes that "Nishitoba et al. fail to disclose the limitation that '*wherein a semiconductor layer of the first transistor continues to a semiconductor layer of the second transistor*'" (page 6, Paper No. 20080718; emphasis in original). The Official Action continues by asserting "i.e. the first and second transistors are formed on the same substrate/semiconductor layer" (Id.; emphasis added). The Applicant notes that the latter assertion is inaccurate in that the present claims recite that a first transistor and a second transistor share a same semiconductor layer, not that that a first transistor and a second transistor share are formed on a same semiconductor layer.

Yudasaka does not cure the deficiencies in Nishitoba. The Official Action asserts that Yudasaka discloses that "[t]he active matrix device comprising at least two thin film transistors (TFT) and an electroluminescent element (EL element)" and "[a]s illustrated by figures 3A and 3B, the first TFT (ref. #20) and the second TFT (ref. #30) on the same semiconductor film (see e.g. col. 5, lines 31-45; col. 9, lines 29-54; fig. 2)" (page 6, Id.;

emphasis added). Again, the Applicant notes that the latter assertion is inaccurate in that the present claims recite that a first transistor and a second transistor share a same semiconductor layer.

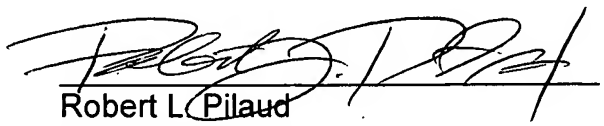
Yudasaka appears to teach that "the first TFT 20 and the second TFT 30 are formed by utilizing island-like semiconductor films" (column 5, lines 32-33; emphasis added). Yudasaka does not teach or suggest that the first TFT 20 and the second TFT 30 could or should share the same semiconductor layer or that Nishitoba should be modified to include such features.

Therefore, the Applicant respectfully submits that Nishitoba and Yudasaka, either alone or in combination, do not teach or suggest that a first transistor and a second transistor share a same semiconductor layer.

Since Nishitoba and Yudasaka do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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